IN THE CLAIMS:

Please cancel claim 12. **Please also amend** claims 1, 8, 17, and 19, and **add** new claims 21-24, as shown in the complete list of claims that is presented below.

1. (currently amended) An information processing apparatus that can perform an interruption function comprising:

a central processing unit that operates with one of a first clock and a second clock, the second clock having a shorter period than the first clock;

a clock generating circuit for generating the second clock upon receiving a start signal;

a clock switching circuit for normally supplying the first clock to the central processing unit to cause the central processing unit to operate with the first clock, and for supplying the second clock, instead of the first clock, to the central processing unit to cause the central processing unit to operate with the second clock when a predetermined condition is present; and

an interrupt control circuit for supplying the start signal substantially simultaneously to both the central processing unit and the clock generating circuit when the interrupt control circuit receives an interrupt request signal, the start signal being supplied to the clock generating circuit without passing through the central processing circuit, the start signal causing the central processing unit to start preparation for the interruption and additionally causing the clock generating circuit to start producing the second clock while the central processing unit is starting preparation for the interruption, so that stabilization of oscillation of the second clock proceeds as the central processing unit is preparing for the interruption.

Claim 2 (cancelled).

3. (previously presented) The information processing apparatus according to claim 1, wherein the predetermined condition is present when the central processing circuit completes the preparation for the interruption, and oscillation of the second clock derived from the clock generating circuit becomes stable.

4. (previously presented) The information processing apparatus according to claim 1, wherein the predetermined condition is present when the longer of a time needed for the central processing circuit to complete the preparation for the interruption and a time needed for clock oscillation to become stable elapses.

5. (original) The information processing apparatus according to claim 1, wherein the central processing unit starts processing interruption data at a high speed upon receiving the second clock.

Claim 6 (cancelled).

7. (previously presented) The information processing apparatus according to claim 1, wherein the start signal is supplied in parallel to the central processing unit and the clock generating circuit.

8. (currently amended) An information processing apparatus that can perform an interruption function comprising:

a central processing unit adapted to operate with a first clock;

a clock generating circuit for generating a second clock upon receiving an interrupt request signal, the second clock having a shorter period than the first clock; and

an interrupt control circuit for storing interruption data in accordance with the second clock, and for supplying a start signal to the central processing unit upon receiving the interrupt request signal, to cause the central processing unit to start preparation ~~of~~ for the interruption and feeding the interruption data to the central processing unit after the central processing unit completes the preparation of the interruption such that the central processing data performs the interruption with the interruption data,

wherein the control processing unit performs the interruption in accordance with the first clock, and

wherein the clock generating circuit and the interrupt control circuit receive the interrupt request signal at substantially the same time, so that stabilization of oscillation of the second clock proceeds as the central proceeding unit is preparing for the interruption.

9. (original) The information processing apparatus according to claim 8, wherein the interrupt control circuit stores the interruption data after supplying the start signal to the central processing unit.

10. (original) The information processing apparatus according to claim 8, wherein the interrupt request signal is supplied to the clock generating circuit without passing through the interrupt control circuit.

11. (original) The information processing apparatus according to claim 8, wherein the second clock has a short period sufficient not to cause an overflow of the interruption data.

Claim 12. (cancelled)

13. (original) The information processing apparatus according to claim 8, wherein the interrupt control circuit stores the interruption data after oscillation of the second clock produced from the clock generating circuit becomes stable.

Claim 14 (cancelled).

15. (original) The information processing apparatus according to claim 8, wherein the preparation of the interruption and generation of the second clock are initiated at substantially the same time.

16. (original) The information processing apparatus according to claim 8, wherein the start signal is supplied to the central processing unit at substantially the same time the interrupt request signal is supplied to the clock generating circuit.

17. (currently amended) An apparatus comprising:

central processing means adapted to operate with one of a first clock and a second clock, the second clock having a shorter period than the first clock;

means for generating the second clock upon receiving a start signal;

means for normally supplying the first clock to the central processing means to cause the central processing means to operate with the first clock, and for supplying the second clock, instead of the first clock, to the central processing means to cause the

central processing means to operate with the second clock when a predetermined condition is present; and

means for supplying the start signal substantially simultaneously to both the central processing means and the second clock generating means upon receiving an interrupt request signal, the start signal causing the central processing means to start preparation for the interruption and additionally causing the means for generating to start producing the second clock while the central processing means is starting preparation for the ~~interrupt.~~ interruption, so that stabilization of oscillation of the second clock proceeds as the central processing means is preparing for the interruption.

Claim 18 (cancelled).

19. (currently amended) An apparatus comprising:

central processing means adapted to operate with a first clock;

means for generating a second clock upon receiving an interrupt request signal, the second clock having a shorter period than the first clock;

means for storing interruption data in accordance with the second clock;

means for supplying a start signal to the central processing means upon receiving the interrupt request signal, to cause the central processing means to start preparation ~~of~~ for the interruption; and

means for feeding the interruption data to the central processing means after the central processing means completes the preparation of the interruption such that the central processing means performs the interruption with the interruption data in accordance with the first clock,

wherein stabilization of oscillation of the second clock proceeds as the central processing means is preparing for the interruption.

20. (original) The apparatus according to claim 19, wherein the means for storing the interruption data stores the interruption data after the means for supplying the start signal supplies the start signal to the central processing means.

21. (new) The information processing apparatus according to claim 1, wherein the central processing unit operates with the first clock during a halt mode and with the

second clock during an operational mode, and switching from the halt mode the operational mode takes place while said stabilization of oscillation of the second clock is proceeding.

22. (new) The information processing apparatus according to claim 8, wherein the central processing unit operates with the first clock during a halt mode and with the second clock during an operational mode, and switching from the halt mode the operational mode takes place while said stabilization of oscillation of the second clock is proceeding.

23. (new) The apparatus according to claim 17, wherein the central processing means operates with the first clock during a halt mode and with the second clock during an operational mode, and switching from the halt mode the operational mode takes place while said stabilization of oscillation of the second clock is proceeding.

24. (new) The apparatus according to claim 19, wherein the central processing means operates with the first clock during a halt mode and with the second clock during an operational mode, and switching from the halt mode the operational mode takes place while said stabilization of oscillation of the second clock is proceeding.